CEN/CLC/JTC 22/WG 3 "Quantum Computing and Simulation"

Convenor: **Paul Alexandra Mme**

Nxxx_WorkItem_TS_on_HAL

Document type	Related content	Document date	Expected action
General / Other		2025-11-24	**INFO**

Description

Dear members,

Please find attached the proposal a TS on Hardware Abstraction Layer.

The proposal is to create a first TS about the “Hardware Abstraction Layer” (HAL), which concentrates on a dedicated layer within TR 18202:2025 (“Layer Model of Quantum Computing”). It aims at creating functional descriptions and functional requirements of relevant functionalities within the HAL.

Kind regards,

New Work Item	
* to be attached to the CIB	
CEN/CENELEC JTC 22/WG3 – Quantum Technologies	
Secretariat: DIN	Proposal documented in N xx
Date of circulation:	Closing date for voting:
Decision reference:	Decision date:

Proposal

0. This proposal relates to

☐ the adoption of a New Work Item in the committee's work programme (stage 10.99)

☒ the adoption of a Preliminary Work Item in the committee's work programme (stage 00.60)

☐ the activation of a Preliminary Work Item in the committee's work programme (stage 10.99):

1. Deliverable

☐ European Standard (EN)

☒ Technical Specification (TS)

☐ Technical Report (TR)

2. This item corresponds to

☒ A new project

☐ An amendment to the EN *XXX*

☐ The revision of EN *XXX*

☐ The conversion of TS *XXX* into an EN *XXX*

☐ The revision of TS *XXX*

☐ The revision of TR *XXX*

2.1 - Only for WIs of CEN/TCs (not applicable to CEN-CLC/JTCs WIs): if this item corresponds to an amendment/revision of
an EN indicate if:

☐ the scope will change (weighted vote required - select the right option in the CIB)

☐ the scope will not change (simple majority vote required - select the right option in the CIB)

3. Explain the purpose and give a justification for this proposal (max 4000 characters). This text should provide information
on technical topics to be discussed.

The proposal is to create a first TS about the "Hardware Abstraction Layer" (HAL), which concentrates on a dedicated layer within TR 18202:2025 ("Layer Model of Quantum Computing"). It aims at creating functional descriptions and functional requirements of relevant functionalities within the HAL

The importance of a Hardware Abstraction Layer in modular quantum computing is rapidly increasing as the ecosystem expands to include hardware and software products from multiple vendors. This growth creates a strong need for a TS that ensures interoperability and portability across diverse quantum platforms. The HAL enables higher-level software and compilers to operate independently of hardware-specific details, allowing customers, such as research institutes and system integrators, to combine components from different vendors into a single, cohesive quantum system. This approach mirrors the success of abstraction layers in classical computing, which fueled the rise of modular architectures and accelerated market adoption. For quantum computing, such modularity can only succeed if the HAL provides well-defined, standardized interfaces that support instruction translation, resource management, and hardware capability reporting. These interfaces must offer access to well-described functionalities within the HAL to guarantee compatibility, scalability, and security across the supply chain. By formalizing these aspects, the HAL becomes a cornerstone for building flexible, vendor-neutral quantum computing stacks.

It is expected that a full specification of the HAL will be developed in parts, where the first part concentrates on functional descriptions and functional requirements only. The word "functional" means within this context that a precise definition of interfaces, information flows (via instructions, commands, signals, etc) and values is out of scope of this first part, and that this first part mainly concentrates on general descriptions of what layers should support and which properties or quantities are to be considered for future specification.

Currently the latest results are in TR 18202:2025, which describes the layer model as a whole. It gives the outline of the hardware abstraction layer in relation to the other layers.

4. Titles

English title: Hardware Abstraction Layer;
Part 1: Descriptions and functional requirements

French title:
(*Optional*)

German title:
(*Optional*)

5. Scope of the proposed work item (max 4000 characters)

This TS defines functional descriptions and requirements for the HAL within the quantum computing software stack, while specific implementation values remain out of scope. The HAL sits between the assembly layer and the control software layer (with an ISA), as described in TR 18202:2025 ("Layer Models for Quantum Computing."). Its purpose is to provide a standardized interface that abstracts away hardware-specific details and exposes essential capabilities to higher layers, enabling portability and interoperability across diverse quantum architectures.

The HAL is designed to support a wide range of quantum hardware platforms, each with unique characteristics such as qubit topology, native gate sets, and error correction schemes. Rather than prescribing strict implementation details, this TS focuses on defining the functionalities of the HAL, including instruction translation, resource management, virtualization for multi-user environments, and reporting of hardware capabilities. These functionalities allow compilers and programming frameworks to optimize execution without requiring direct interaction with proprietary hardware interfaces.

This "Part 1" of the TS is structured to accommodate future developments and revisions, leaving detailed specifications of interfaces and parameter values for subsequent parts. It is not necessary to describe all possible hardware architectures before publishing this part; however, it must provide sufficient detail to enable higher layers to be standardized in complementary documents. By establishing these foundational requirements, the HAL becomes a cornerstone for modular quantum computing systems, ensuring flexibility, scalability, and vendor-neutral integration.

6. Digital aspects

☒ The deliverable is intended to be developed using the Online Collaborative Authoring platform

☐ The deliverable is intended to include non-Word/PDF content, e.g. audio files, XML schemas, machine-readable formats or software.
Please provide details of the non-Word/PDF content:

☐ None of the above.

If yes to either of these questions, CCMC will contact you for feasibility and organizational aspects.

7. Stakeholder categories immediately affected by the proposal

☒ Industry and commerce	☐ Societal consumer groups	☒ Standards application
☒ SMEs	☐ Labour	☐ Non-governmental organization (NGO)
☒ Government	☒ Academic and research bodies	☐ Environmental stakeholders
☐ Consumers		
☐ None of the above categories		

8. How will these Stakeholders benefit from or be impacted by the proposed deliverable?

The market for software components and abstraction layers in quantum computing is expanding rapidly as multiple vendors develop hardware and software solutions for diverse architectures. Research institutions, system integrators, and technology companies increasingly require standardized interfaces to enable interoperability and portability across these heterogeneous systems. This demand highlights the need for a TS dedicated to the HAL, which serves as the bridge between higher-level programming environments and vendor-specific hardware implementations.

The HAL is essential for modular quantum computing because it allows customers to integrate products from different vendors into a unified system without being locked into proprietary solutions. By abstracting hardware-specific details and providing a common interface for instruction translation, resource management, and hardware capability reporting, the HAL enables compilers and software frameworks to operate seamlessly across multiple platforms. Standardization of the HAL will

benefit all stakeholders: customers can clearly communicate their requirements, and vendors can deliver modules that interoperate reliably within a global ecosystem. This approach fosters a scalable and competitive market, similar to the modularity that drove the success of classical computing. Establishing functional descriptions and requirements for the HAL in this TS is the first step toward achieving that vision, paving the way for future parts that will define strict interface specifications and compliance criteria.

9. Document developed in drafting body

☒ Existing drafting body *(please give name and title)*:

☐ New drafting body *(please give name and title)*:
Proposal for addressing the hardware abstraction layer,
CEN-CLC-JTC 22-WG 3_Nxxx_Proposal HAL.pdf

10. Proposed Project Leader (including contact details) - *Optional*

Rob F.M. van den Brink – Netherlands – Rob.vandenBrink@Delft-Circuits.com

11. United Nations Sustainable Development Goals (SDGs)

Please select any United Nations Sustainable Development Goals (SDGs) that this document will support. For more information, please visit the SDG section of the CEN website (currently under development).

☐ GOAL 1: No Poverty
☐ GOAL 2: Zero Hunger
☐ GOAL 3: Good Health and Well-being
☐ GOAL 4: Quality Education
☐ GOAL 5: Gender Equality
☐ GOAL 6: Clean Water and Sanitation
☐ GOAL 7: Affordable and Clean Energy
☐ GOAL 8: Decent Work and Economic Growth
☒ GOAL 9: Industry, Innovation and Infrastructure
☐ GOAL 10: Reduced Inequality
☐ GOAL 11: Sustainable Cities and Communities
☐ GOAL 12: Responsible Consumption and Production
☐ GOAL 13: Climate Action
☐ GOAL 14: Life Below Water
☐ GOAL 15: Life on Land
☐ GOAL 16: Peace and Justice Strong Institutions (N/A GOAL 17: Partnerships to achieve the Goal)
☐ None of the above

Proposed rationale for the selected SDG(s)- (optional):

12. Accessibility aspects

See CEN-CENELEC Guide 6:2014 'Guide for addressing accessibility in standard'

☐ Accessibility aspects are relevant for this NWI *(please indicate which ones):*

See the 'protocol' to help you decide when accessibility following a Design for All approach is relevant:
https://www.cencenelec.eu/areas-of-work/cen-cenelec-topics/accessibility/design-for-all/

☒ Accessibility aspects are not relevant for this NWI

Please provide a written explanation detailing why accessibility aspects do not apply to the current proposed WI:

The deliverable itself is a TS, developed in an accessible way like any other CEN-CENELEC TS. The content of the TS will not affect any accessibility aspects (i.e. 24x "no" to the questions from "The Protocol Form")

13. Environmental aspects

☐ Discharges to soil	☐ Discharges to water	☐ Emission to air
☐ Heat	☐ Noise/Vibration	☐ Use of land
☐ Radiation	☒ Use of energy	☐ Other effects on biodiversity
☒ Use of material	☐ Use of water	☐ Waste
☐ Risk to the environment from accidents/misuse		☐ Chemicals

☐ Other:

☐ None of the above.

Please provide a written explanation detailing why these environmental aspects do not apply to the current proposed WI:

14. How do you plan to address these environmental aspects?

☐ Bring in environmental expertise to the WG

☐ Contact EHD for help/support (cen.ehd@cencenelec.eu) and/or use examples from Environmental Framework
https://www.cencenelec.eu/areas-of-work/cen-cenelec-topics/environment-and-sustainability/environmental-helpdesk-and-trainings/

☐ Use of environmental checklist and guides (please visit the dedicated section in the CEN website

☒ Other:

Environment aspects are included as part of the analysis, e.g. energy use.?????

15. Vienna Agreement (parallel procedure)

☒ No or Vienna Agreement with CEN lead proposed

The project focusses on the European perspective. There does not exist a parallel ISO activity on this particular topic/scope of the project.

☐ Yes – Vienna Agreement Parallel with ISO

Lead ISO project reference:

ISO project

ID: ISO/TC:

16. The project is based on

☒ No document from another organization
It is a natural follow-up from TR 18202:202 (Layer Model for Quantum Computing), written within CEN-CENELEC JTC22/WG3, and published in October 2025

☐ An ISO or ISO/IEC document (not covered by a parallel procedure)

☐ Identical

☐ Non-identical

ISO/IEC project reference:
ISO/IEC project ID:
Publication date:

☐ A document from another organization than ISO or ISO /IEC:

Note: Please explain the purpose and give a justification for this proposal in Section 3.

☒ The project will make reference to relevant standards from ISO/IEC, ITU-T, ETSI, NIST and other.

17. Please indicate whether the proposed project is linked to a specific European Research and Innovation Project

☐ No

☒ Yes

Research and/or Innovation project code:
Research and/or Innovation project acronym: QUCATS
Research and/or Innovation project title:

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Research and/or Innovation project acronym:
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Research and/or Innovation project acronym:
Research and/or Innovation project title:

To do: plenty of Europeans projects working on Quantum Computing.

18. Track

☐ Enquiry + Formal Vote (for EN)

☒ Vote on TS or TR by correspondence

19. Please provide the target dates for the below key stages.

19.1 – For ENs

N/A

19.2 – For TSs and TRs

Project start date (10.99)	~~Dispatch of 1st WD (20.60)~~	Dispatch of draft for Vote (30.99)
2025-12-01	2026-01-26	2026-08-25

20. Related standardization request(s) (formerly mandate):

☒ No

☐ Yes *(please specify)*:

21. Related directive(s)/regulation(s)

☒ No

	Directive/ Regulation reference	Candidate for citation in Official Journal?
□ Yes		☐ No ☐ Yes
		☐ No ☐ Yes

22. Relation to other legislation or established public policy.

☒ No

☐ Yes

Please specify which legislation or established public policy is/are in relation with the proposed project:

23. Is the proposed project covered by Intellectual Property Rights (IPR)?

Please indicate whether there is any knowledge of items covered by IPR(s), for instance patents, copyright, trademark, etc.

☒ No

☐ Yes

Please provide full information about these items and the identified IPR(s):

24. Commitment This section applies only to *CEN-CLC/JTC* T*o be completed for NWI request to be approved by CEN and CENELEC BTs.*

The following members (at least five) are committed to participate in the development of the project:

1) Netherlands (contact: juan.boschero@tno.nl)
2) Italy
3) Germany
4) Austria
5)